Power MOSFET

Zheng Yang

(ERF 3017, email: yangzhen@uic.edu)
Evolution of low-voltage (<100V) power rectifiers

Chapter 5 in textbook; discussed.

Chapter 4 in textbook; discussed.

Not covered by this textbook; did NOT discuss.

Not covered by this textbook; did NOT discuss.

(JBS: junction barrier controlled Schottky)

(TMBS: trench MOS barrier rectifier Schottky)

Evolution of high-voltage (>300V) power rectifiers

Chapter 5 in textbook; discussed.

Not covered by this textbook; did NOT discuss.

Covered by this textbook briefly (Section 4.4.4); discussed very briefly.

(MPS: merged P-i-N and Schottky)

Evolution of power MOSFET structures

Chapter 6 in textbook; will discuss.
Chapter 6 in textbook; will discuss.
Chapter 6 in textbook; will discuss.
Not covered by this textbook; will NOT discuss.

Power MOSFET Background

The vertical power metal-oxide-semiconductor field effect transistor (MOSFET) structure was developed in the mid-1970s to obtain improved performance when compared with the existing power bipolar transistors. One of the major issues with the power bipolar transistor structure was its low-current gain when designed to support high voltages. In addition, power bipolar transistors could not be operated at high frequencies due to the large storage time related to the injected charge in their drift regions and were prone to destructive failure during hard switching in applications with inductive loads. The replacement of these current-controlled devices with a voltage-controlled device was attractive from an application’s viewpoint. The high input impedance of the metal-oxide-semiconductor (MOS)-gate structure simplified the drive circuit requirements when compared with bipolar transistors being used at that time. In addition, their superior switching speed opened new applications operating in the 10–50 kHz frequency domain. Today, power MOSFETs are the most commonly used power switches in applications where the operating voltages are below 200 V.

The vertical power MOSFETs were initially considered to be ideal power switches due to their high input impedance and fast switching speed. However, their power-handling capability was constrained by the internal resistance within the structure between the drain and source electrodes. The power dissipated due to the Ohmic voltage drop in the internal resistance limited the current-handling capability of the power MOSFETs as well as the efficiency of the power circuits in which they were utilized.
MOS Interface Physics—Flat Band Conditions

\[ q\phi_M = q\chi_S + \frac{E_G}{2} + q\psi_B = q\phi_B + q\chi_O, \]

\[ \psi_B = \left( \frac{E_i - E_{FS}}{q} \right) = \frac{kT}{q} \ln \left( \frac{p_0}{n_i} \right) \]
MOS Interface Physics—Accumulation Conditions
MOS Interface Physics—Depletion Conditions

Metal | Oxide | Semiconductor

$V_G > 0$

$E_{FM}$

$E_C$

$E_i$

$E_{FS}$

$E_V$
MOS Interface Physics—Inversion Conditions

![Diagram showing MOS interface physics with labels for metal, oxide, and semiconductor regions, energy levels EC, EI, EF, and EV, and the condition VG > 0.]
MOS Surface Charge Analysis

\[ \frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\varepsilon_S} \]

\[ \rho(x) = q\left(N_D^+ - N_A^- + p_P - n_P\right) \]
MOS Surface Charge Analysis (cont’d)

\[
\frac{d^2 \psi}{dx^2} = -\frac{\rho(x)}{\varepsilon_S}
\]

\[
\rho(x) = q(N_D^+ - N_A^- + p_p - n_p).
\]

\[
n_p = n_{p0}e^{q\psi/kT}, \quad p_p = p_{p0}e^{-q\psi/kT}, \quad N_D^+ - N_A^- = n_{p0} - p_{p0}
\]

\[
\frac{d^2 \psi}{dx^2} = -\frac{q}{\varepsilon_S} [p_{p0}(e^{q\psi/kT} - 1) - n_{p0}(e^{q\psi/kT} - 1)]
\]

\[
E(x) = -\frac{d\psi}{dx} = \frac{\sqrt{2kT}}{qL_D} F\left(\frac{q\psi}{kT}, \frac{n_{p0}}{p_{p0}}\right)
\]

\[
L_D = \sqrt{\frac{kT\varepsilon_S}{q^2p_{p0}}}
\]

\[
F\left(\frac{q\psi}{kT}, \frac{n_{p0}}{p_{p0}}\right) = \left\{\left[e^{-q\psi/kT} + \left(\frac{q\psi}{kT}\right) - 1\right] + \frac{n_{p0}}{p_{p0}}\left[e^{q\psi/kT} - \left(\frac{q\psi}{kT}\right) - 1\right]\right\}^{1/2}
\]

\[
Q_s = -\varepsilon_S E_s = \frac{\sqrt{2\varepsilon_S kT}}{qL_D} F\left(\frac{q\psi_s}{kT}, \frac{n_{p0}}{p_{p0}}\right)
\]
MOS Surface Charge Analysis (cont’d)

\[ Q_s = \frac{\sqrt{2 \varepsilon_S kT}}{qL_D} F\left(\frac{q\psi_S}{kT}, \frac{n_{p0}}{p_{p0}}\right) \]

Diagram:
- **Accumulation**
- **Strong Inversion**
- **Depletion**
- **Weak Inversion**

**Doping Concentration = 1 \times 10^{16} \text{ cm}^{-3}**

**Surface Charge (C/cm^2):**
- 10^{-6}
- 10^{-7}
- 10^{-8}
- 10^{-9}

**Surface Potential (Volts):**
- -0.2
- -0.1
- 0
- 0.1
- 0.2
- 0.3
- 0.4
- 0.5
- 0.6
- 0.7
- 0.8
- 0.9

**Symbols:**
- \( E_v \)
- \( E_f \)
- \( E_i \)
- \( E_c \)
- \( \psi_B \)
- \( 2\psi_B \)
MOS Surface Charge Analysis (cont’d)

\[ Q_s(\text{accumulation}) = \frac{\sqrt{2e_s kT}}{qL_D} e^{-\frac{q\psi_S}{2kT}} \]

\[ Q_s(\text{depletion}) = \frac{e_s}{L_D} \sqrt{\frac{2kT}{q}} \psi_S = \sqrt{2q e_s p_{p0} \psi_S} \]

\[ Q_s(\text{weak inversion}) = \sqrt{2q e_s p_{p0} \psi_S} \]

\[ Q_s(\text{strong inversion}) = \frac{\sqrt{2e_s kT}}{qL_D} \sqrt{\frac{n_{p0}}{p_{p0}}} e^{q\psi_S/2kT} = \sqrt{2e_s kT n_{p0}} e^{q\psi_S/2kT} \]
Maximum Depletion Width

\[ W_M = \sqrt{\frac{2 \varepsilon_S}{q N_A}} (2 \psi_B) \]

\[ W_M = \sqrt{\frac{4 \varepsilon_S kT}{q^2 N_A}} \ln \left( \frac{N_A}{n_i} \right) \]
Threshold Voltage

\[
V_{TH} = \frac{Q_s}{C_{OX}} + 2\psi_B = \frac{\sqrt{2\varepsilon_S n_{p0}}}{C_{OX}} e^{\frac{q\psi_B}{kT}} + 2\psi_B = \frac{\sqrt{4\varepsilon_S kT N_A \ln(N_A/n_i)}}{C_{OX}} + \frac{2kT}{q} \ln\left(\frac{N_A}{n_i}\right)
\]

Graph showing the relationship between threshold voltage and oxide thickness for different doping concentrations. The graph plots threshold voltage (Volts) against oxide thickness (Angstroms) with doping concentrations of \(1 \times 10^{15}\), \(1 \times 10^{16}\), \(1 \times 10^{17}\), and \(1 \times 10^{18}\) cm\(^{-3}\) as labels.
Threshold Voltage (work function difference)

\[ q\phi_{MS} = q\phi_B + q\chi_O - (q\chi_S + E_i + q\psi_B) \]
Threshold Voltage (oxide charge)

\[ V_{TH} = \sqrt{4\varepsilon_s kT N_A \ln\left(\frac{N_A}{n_i}\right)} + \frac{2kT}{q} \ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{OX}}{C_{OX}} \]

Gate Oxide = 500 Angstroms; N\textsuperscript{+} Polysilicon

Oxide Charge (cm\textsuperscript{-2})

Zero

1 x 10\textsuperscript{11}

2 x 10\textsuperscript{11}

5 x 10\textsuperscript{11}

1 x 10\textsuperscript{12}

(n-channel)
Threshold Voltage (oxide charge)

\[
V_{TH} = \sqrt{4\varepsilon_S k T N_A \ln\left(\frac{N_A}{n_i}\right)} + \frac{2kT}{q} \ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{ox}}{C_{ox}}
\]

(p-channel)
MOSFET Channel Resistance

V_D << (V_G - V_TH)

V_D = (V_G - V_TH)

V_D > (V_G - V_TH)
MOSFET Channel Resistance (cont’d)

\[ Q_n = C_{OX} (V_G - V_{TH}) \]

\[ R_{CH} = \frac{L_{CH}}{Z \mu_{ni} C_{OX} (V_G - V_{TH})} \]

\[ dR = \frac{dx}{Z \mu_{ni} Q_n (x)} \]

\[ Q_n (x) = C_{OX} [V_G - V_{TH} - V(x)] \]

\[ dV = I_D dR \]

\[ \int_{0}^{L_{CH}} I_D dx = Z \mu_{ni} C_{OX} \int_{0}^{V_D} (V_G - V_{TH} - V) dV \]

\[ I_D = \frac{Z \mu_{ni} C_{OX}}{2L_{CH}} [2(V_G - V_{TH})V_D - V_D^2] \]

\[ V_P = V_G - V_{TH} \]

\[ I_D = \frac{Z \mu_{ni} C_{OX}}{L_{CH}} [(V_G - V_{TH})V_D] \]

\[ R_{CH} = \frac{V_D}{I_D} = \frac{L_{CH}}{Z \mu_{ni} C_{OX} (V_G - V_{TH})} \].
The first high-voltage power MOSFET structure was developed by using a V-groove etching process during the 1970s. A cross section of this V-MOSFET structure is illustrated in the left hand side figure. The N+ source and drain regions in the vertical power MOSFET structure are separated by a P-base region, resulting in the formation of two P-N junctions labeled J1 and J2 in the figure. A V-groove is formed at the upper surface that penetrates through both the junctions. The gate electrode is placed inside the V-groove after creating a gate oxide on its surface, preferably by thermal oxidation of the silicon.

Without the application of a gate bias, junction J1 becomes reverse biased when a positive bias is applied to the drain electrode. A high voltage can be supported under these conditions by appropriate choice of the doping concentration and thickness of the N-drift region. The second junction J2 is short circuited by overlapping the source electrode over the junction as illustrated in the figure to suppress the parasitic bipolar transistor. With proper design considerations, the breakdown voltage approaches that for a P-N diode. Current flow between the drain and source electrodes of the V-MOSFET structure can be induced by the formation of a channel at the surface of the P-base region below the gate oxide. A positive bias applied to the gate electrode attracts electrons to the semiconductor surface under the gate oxide. These electrons provide a path for current flow between the source and the drain. The maximum current carrying capability is determined by the internal resistance within the structure. A smaller resistance can be achieved by using smaller dimensions in the cell structure to increase the channel density.
The V-MOSFET structure fell out of favor because of manufacturing difficulties. The V-groove was formed by using a potassium hydroxide-based etch for silicon, which exhibits different etch rates for various silicon surface orientations. It was found that the potassium from the etch solutions contaminates the gate oxide, producing instabilities during long-term operation of the V-MOSFET structure. In addition, the sharp corner at the bottom of the V-groove was found to degrade the breakdown voltage.
D-MOSFET (or VD-MOSFET)

Note: Different books sometimes use different names of this type of power MOSFET. The names *VD-MOSFET, vertical-diffused MOSFET, double-diffused MOSFET, and DMOSFET* refer to the exactly same device structure.
A cross section of the basic cell structure for the DMOSFET is illustrated in above figure. This device structure is fabricated by starting with an N-type epitaxial layer grown on a heavily doped N+ substrate. The channel is formed by the difference in lateral extension of the P-base and N+ source regions produced by their diffusion cycles. Both regions are self-aligned to the left-hand side and right-hand side of the gate region during ion implantation to introduce the respective dopants. A refractory gate electrode, such as polysilicon, is required to allow diffusion of the dopants under the gate electrode at elevated temperatures.
How a D-MOSFET works?

Without the application of a gate bias, a high voltage can be supported in the D-MOSFET structure when a positive bias is applied to the drain. In this case, junction $J_1$ formed between the P-base region and the N-drift region becomes reverse biased. The voltage is supported mainly within the thick lightly doped N-drift region. Drain current flow in the D-MOSFET structure is induced by the application of a positive bias to the gate electrode. This produces an inversion layer at the surface of the P-base region under the gate electrode. This inversion layer channel provides a path for transport of electrons from the source to the drain when a positive drain voltage is applied.
How a D-MOSFET works? (cont’d)

After transport from the source region through the channel, the electrons enter the N-drift region at the upper surface of the device structure. They are then transported through a relatively narrow JFET region located between the adjacent P-base regions within the D-MOSFET structure. The constriction of the current flow through the JFET region substantially increases the internal resistance of the D-MOSFET structure. A careful optimization of the gate width ($W_G$) is required to minimize the internal resistance for this structure. In addition, it is customary to enhance the doping concentration in the JFET region to reduce the resistance to current flow through this portion of the device structure.

After being transported through the JFET region, the electrons enter the N-drift region below junction $J_1$. The current spreads from the relatively narrow JFET region to the entire width of the cell cross section. This non-uniform current distribution within the drift region increases its resistance, making the internal resistance of the D-MOSFET structure larger than the ideal specific on-resistance of the drift region. The large internal resistance for the D-MOSFET structure provided motivation for the development of the trench-gate power MOSFET structure in the 1990s.
D-MOSFET On-Resistance

Source Contact Resistance $R_{CS}$
Source Region Resistance $R_{N^+}$
Channel Resistance $R_{CH}$
Accumulation Resistance $R_A$
JFET Resistance $R_{JFET}$
Drift Region Resistance $R_D$
Substrate Resistance $R_{SUB}$
Drain Contact Resistance $R_{CD}$

$$R_{ON} = R_{CS} + R_{N^+} + R_{CH} + R_A + R_{JFET} + R_D + R_{SUB} + R_{CD}.$$
D-MOSFET On-Resistance (cont’d)

Source Contact Resistance $R_{CS}$

Source Region Resistance $R_{N+}$

Channel Resistance $R_{CH}$

Accumulation Resistance $R_{A}$

JFET Resistance $R_{JFET}$

Drift Region Resistance $R_{D}$

Substrate Resistance $R_{SUB}$

Drain Contact Resistance $R_{CD}$: smaller comparing to the Source Contract Resistance $R_{CS}$
### D-MOSFET On-Resistance (cont’d)

<table>
<thead>
<tr>
<th>Resistance</th>
<th>Value (mOhm-cm²)</th>
<th>Percentage Contribution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source Contact ($R_{CS,SP}$)</td>
<td>0.05</td>
<td>2.2</td>
</tr>
<tr>
<td>Source ($R_{N+,SP}$)</td>
<td>0.01</td>
<td>0.4</td>
</tr>
<tr>
<td>Channel ($R_{CH,SP}$)</td>
<td>0.92</td>
<td>41.0</td>
</tr>
<tr>
<td>Accumulation ($R_{A,SP}$)</td>
<td>0.66</td>
<td>29.5</td>
</tr>
<tr>
<td>JFET ($R_{JFET,SP}$)</td>
<td>0.19</td>
<td>8.5</td>
</tr>
<tr>
<td>Drift ($R_{D,SP}$)</td>
<td>0.34</td>
<td>15.2</td>
</tr>
<tr>
<td>Substrate ($R_{SUB,SP}$)</td>
<td>0.06</td>
<td>2.7</td>
</tr>
<tr>
<td>Drain Contact ($R_{DS,SP}$)</td>
<td>0.01</td>
<td>0.4</td>
</tr>
<tr>
<td><strong>Total ($R_{T,SP}$)</strong></td>
<td><strong>2.24</strong></td>
<td><strong>100</strong></td>
</tr>
</tbody>
</table>

\[
R_{ON} = R_{CS} + R_{N+} + R_{CH} + R_{A} + R_{JFET} + R_{D} + R_{SUB} + R_{CD}.
\]
During the late 1980s, the technology for etching trenches in silicon became available due to its application for making charge storage capacitors within DRAM chips. This process was adapted by the power semiconductor industry to develop the trench-gate or U-MOSFET structure. As shown in figure above, the trench extends from the upper surface of the structure through the N+ source and P-base regions into the N-drift region. The gate electrode is placed within the trench after the formation of the gate oxide by thermal oxidation of the bottom and sidewalls.
How a U-MOSFET works?

Without the application of a gate bias, a high voltage can be supported in the U-MOSFET structure when a positive bias is applied to the drain. In this case, junction J₁ formed between the P-base region and the N-drift region becomes reverse biased. The voltage is supported mainly within the thick lightly doped N-drift region. Since the gate is at zero potential during the blocking mode of operation, a high electric field is also developed across the gate oxide. To avoid reliability problems arising from the enhanced electric field in the gate oxide at the trench corners, it is customary to round the bottom of the trench.

Drain current flow in the U-MOSFET structure is induced by the application of a positive bias to the gate electrode. This produces an inversion layer channel at the surface of the P-base region along the vertical sidewalls of the trench. This inversion layer channel provides a path for transport of electrons from the source to the drain when a positive drain voltage is applied. After transport from the source region through the channel, the electrons enter the N-drift region at the bottom of the trenches. The current then spreads to the entire width of the cell cross section. Consequently, **there is no JFET region in the U-MOSFET structure, enabling a significant reduction of the internal resistance when compared with the D-MOSFET structure.** The reduced internal resistance for the U-MOSFET structure provided motivation for the development of these devices in the 1990s.
U-MOSFET On-Resistance

Source Contact Resistance $R_{CS}$

Source Region Resistance $R_{N+}$

Channel Resistance $R_{CH}$

Accumulation Resistance $R_{A}$

Drift Region Resistance $R_{D}$

Substrate Resistance $R_{SUB}$

Drain Contact Resistance $R_{CD}$

$$R_{ON} = R_{CS} + R_{N+} + R_{CH} + R_{A} + R_{D} + R_{SUB} + R_{CD}.$$
U-MOSFET On-Resistance (cont’d)

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</tr>
<tr>
<td>Source ((R_{N+,SP}))</td>
<td>0.00005</td>
<td>0.0</td>
</tr>
<tr>
<td>Channel ((R_{CH,SP}))</td>
<td>0.229</td>
<td>37.4</td>
</tr>
<tr>
<td>Accumulation ((R_{A,SP}))</td>
<td>0.055</td>
<td>9.0</td>
</tr>
<tr>
<td>Drift ((R_{D,SP}))</td>
<td>0.209</td>
<td>34.1</td>
</tr>
<tr>
<td>Substrate ((R_{SUB,SP}))</td>
<td>0.06</td>
<td>9.8</td>
</tr>
<tr>
<td>Drain Contact ((R_{DS,SP}))</td>
<td>0.01</td>
<td>1.6</td>
</tr>
<tr>
<td>Total ((R_{T,SP}))</td>
<td>0.613</td>
<td>100</td>
</tr>
</tbody>
</table>

\[ R_{ON} = R_{CS} \cdot R_{N^+} \cdot R_{CH} \cdot R_{A} \cdot R_{D} \cdot R_{SUB} \cdot R_{CD}. \]
## On-Resistance: U-MOSFET vs D-MOSFET

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Summary

The physics of operation of the power MOSFET structure has been discussed in this chapter. The evolution of the device structural design from the planar-gate D-MOSFET architecture to the trench-gate power U-MOSFET architecture has allowed significant reduction of the specific on-resistance, especially for devices designed to support low blocking voltages.

The device structures and working principles of power V-MOSFET, D-MOSFET, and U-MOSFET are discussed. The on-state resistance of D-MOSFET and U-MOSFET are discussed and compared.

Sections discussed: 6.1, 6.2, 6.5, 6.8, 6.23

Sections not discussed: 6.3, 6.4, 6.7, 6.9-6.22