Primary-Side-Converter-Assisted Soft-Switching Scheme for an AC/AC Converter in a Cycloconverter-Type High-Frequency-Link Inverter

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***Abstract*—Emerging trends of high-power-density power-electronics interfaces for renewable- and alternative-energy sources have led to the need for high-frequency-inverter designs without compromising energy-conversion efficiency. In that context, a zero-voltage-switching (ZVS)-based scheme is described in this letter, for a cycloconverter-type high-frequency-link inverter, which is applicable for renewable- and alternative-energy sources as well as other commercial applications. The proposed scheme achieves the primary-side-converter-assisted switching of the ac/ac converter switches under ZVS condition. The modes of operation of the ac/ac converter are explained to outline the behavioral response. The results on the efficacy of the ZVS-based inverter and its performance show satisfactory performances.**

***Index Terms*—AC/AC converter, alternative, cycloconverter, energy sources, fuel cell, high frequency, high-frequency link, inverter, photovoltaic, renewable, zero voltage switching (ZVS).**

I. Introduction

HIGH EFFICIENCY, low cost, and high power density are important attributes of inverters for applications, including distributed-generation systems with renewable- and alternative-energy sources (e.g., photovoltaics, wind, and fuel cells), energy-storage systems, vehicle-to-grid applications, electric/hybrid-electric/fuel-cell vehicles, compact power conversion modules for naval, space, and aerospace applications, and battery-based uninterruptible power supplies. In such systems, galvanic isolation is often required for safety concerns and voltage and current scalabilities. In that regard, a high-frequency-transformer-based approach can be a preferable choice from the standpoint of weight, footprint, and cost reduction. Among the possible topologies, a high-frequency-link (HFL) pulsewidth-modulated (PWM) inverter can eliminate the intermediate LC filter that is needed for a conventional high-frequency (HF) fixed-dc-link converter approach [1]–[3]. Furthermore, as compared to a resonant-link inverter, an HFL inverter yields lower switch stress, better total harmonic distortion (THD), and simpler all-device structure (i.e., no passive components within the power stages). Thus, the PWM HFL inverter approach is better suited from the viewpoints of cost, efficiency, and portability.

Two typical HFL inverter topologies have been proposed in the literature. One is a rectifier-type HFL (RHFL) inverter. It comprises a primary-side HF dc/ac converter feeding an HF transformer, which is followed by an ac/dc converter and a pulsating-dc/ac converter. Thus, the RHFL inverter topology possesses a structure similar to that of a conventional fixed-dc-link inverter except for the absence of the dc-link filter [4]–[9]. One of the features of the RHFL inverter topology is that the input signal to the output ac/ac stage is pulsating dc in nature (with encoded information of the primary-side HF dc/ac converter) that can be used to modulate the ac/ac stage with reduced switching loss [9].

The other class of topology is a cycloconverter-type HFL (CHFL) inverter, as illustrated in Fig. 1, which reduces the conversion complexity by directly placing an ac/ac converter to the secondary side of an HF transformer [10]–[23], which is fed by a primary-side HF dc/ac converter. In the CHFL topology, because the output stage is a single stage, the input to the ac/ac converter is an HF bipolar ac signal generated by the primary-side dc/ac converter. Therefore, switching the ac/ac converter using this primary-side converter information for switching loss reduction is a possibility. One such zero-voltage-switching (ZVS) mechanism, leading to reduced-loss switching with the assistance of a primary-side dc/ac converter, is outlined next in this *letter* which can be extended to a higher number of phases following the same principle.

II. Principle of the ZVS Scheme

With reference to the CHFL inverter illustrated in Fig. 1, Figs. 2 and 3 show two switching schemes (for the ac/ac converter) that will be referred to as the "*conventional scheme*" and the *new* "*ZVS scheme*." The operation of the HF full-bridge dc/ac converter (which remains the same for both the schemes), along with the operation of the conventional scheme, is described in detail in [18] and [22] and is not repeated in

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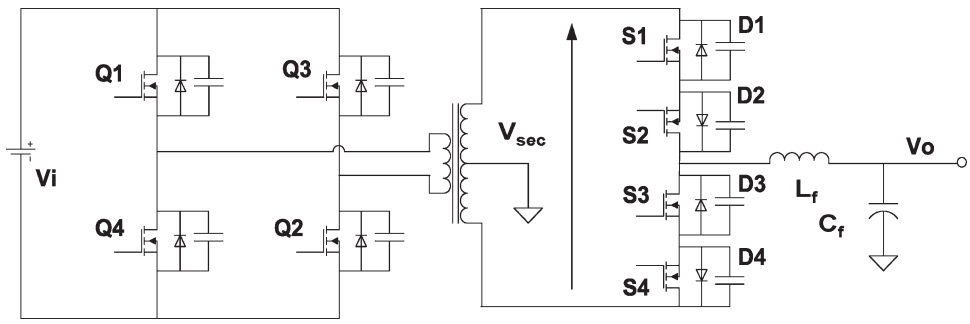

Fig. 1. CHFL inverter comprising a dc/ac and an ac/ac converter on the primary and secondary sides of the HF transformer.

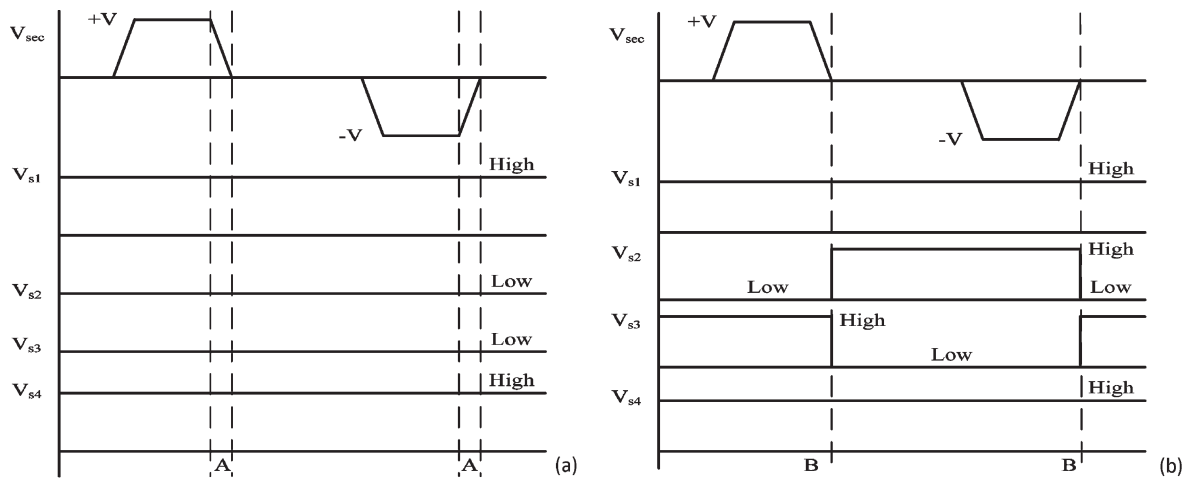

Fig. 2. Gating signals of the ac/ac converter for the "conventional scheme" when the polarities of the output voltage and output current are (a) the same and (b) opposite. The illustration in (a) is for positive output voltage and positive output current. The switching states are complementary if the output voltage and current are both negative. The illustration in (b) is for positive output voltage and negative output current. If the output voltage is negative and the output current is positive, the switching states will be complementary. The symbols L and H represent low and high switching states while $+V$ and $-V$ represent the minimum and maximum voltages of $V_{\rm sec}$, which can be different from V_i.

this letter. The dc/ac converter produces an HF bipolar voltage $(V_{\rm sec})$ across the transformer using sinusoidal pulsewidth modulation. Bipolar voltage is required per switching cycle to ensure transformer flux balance.

For the conventional scheme and as illustrated in Fig. 2, the ac/ac converter has two operating scenarios: one with the polarities of the output voltage and output current being the same and the other with the polarities of the output voltage and output current being opposite. This is explained in detail in [20]. For the first scenario, the ac/ac converter switches operate at line frequency with the antiparallel diodes switching at HF (e.g., in the interval marked "A" in Fig. 2(a) in which the diodes turn off). For the second scenario, the half-bridge ac/ac-converter switches operate at HF [e.g., in the interval marked "B" in Fig. 2(b)] yielding higher switching loss.

For the ZVS scheme, the operating modes (for positive inverter output current and voltage, $V_{\rm sec} \geq 0$, and $V_{\rm sec} \leq 0$) of the ac/ac converter are shown in Fig. 4, along with the switching sequences, which are shown in Fig. 3. The primary-side dc/ac converter dynamics is not illustrated. However, the voltage across the transformer secondary ($V_{\rm sec} = 0$ or $V_{\rm sec} > 0$) demonstrates that the primary-side dc/ac converter is operating in either the zero state or the active state. It is also noted that, even though the output of the dc/ac converter is bipolar, the principle of operation of the ZVS scheme does not change for negative primary-side voltage output. The operating modes are discussed below.

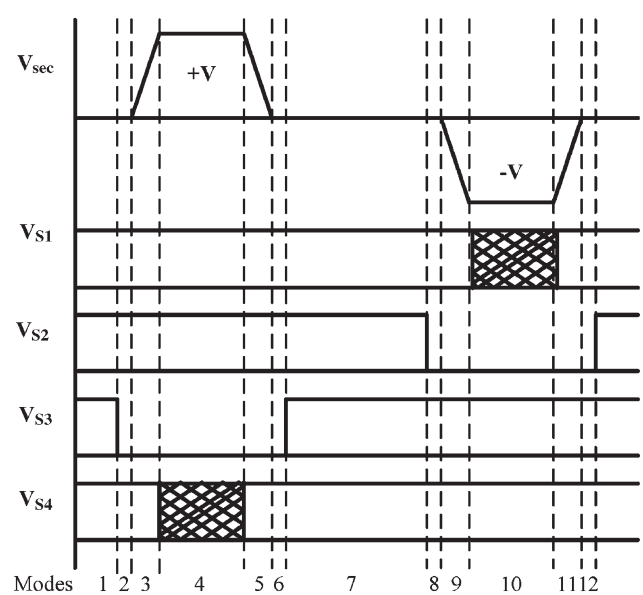

Fig. 3. Gating signals of the ac/ac converter for the "ZVS scheme" when the bipolar transformer secondary voltage is positive/negative.

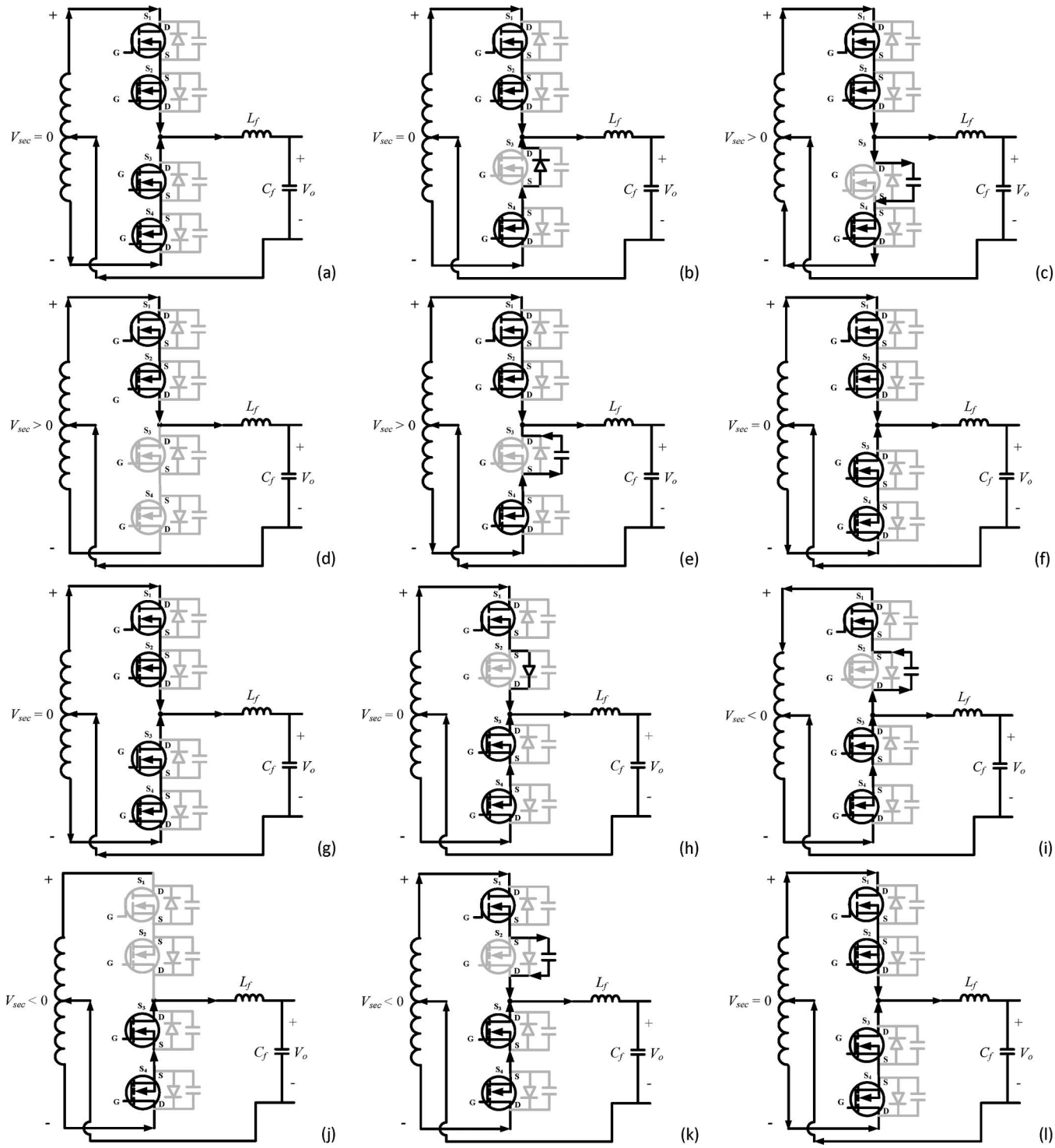

Fig. 4. Operating modes of the ac/ac converter for positive inverter output current and voltage using the dc/ac-converter-assisted ZVS scheme. (a)–(f) $V_{\rm sec} \geq 0$. (g)–(l) $V_{\rm sec} \leq 0$.

Mode 1: In this mode, $V_{\rm sec} = 0$. All of the ac/ac-converter switches are turned on. As such, the output current is shared equally between the two arms of the half-bridge ac/ac converter. Note that the current sharing between the two arms results in lower conduction loss.

Mode 2: This is a zero-state interval during which $V_{\rm sec} = 0$. At the beginning of Mode 2, the switch S_3 is turned off under ZVS condition. Half of the output current that was flowing through the lower arm now begins to transfer to the upper arm. Eventually, the switches S_1 and S_2 carry the output current.

Mode 3: This mode initiates when $V_{\rm sec}$ rises from zero voltage to the dc-bus level and ends with switch S_3 blocking $V_{\rm sec}$.

Mode 4: In this mode, switches S_1 and S_2 support the output current. Because switch S_3 blocks $V_{\rm sec}$, switch S_4 can remain on, or it can be turned off under zero-current condition.

Mode 5: This mode initiates when the primary-side dc/ac converter attains a zero state, and as such, $V_{\rm sec}$ approaches zero voltage. The output current is primarily supported by switches S_1 and S_2 while the output capacitance of switch S_3 discharges, and eventually, it is clamped by the antiparallel diode of S_3.

Mode 6: Similar to Mode 1, this is a zero-state interval. This mode ends when switch S_3 turns on under ZVS condition. Subsequently, the output current is shared between the two arms of the ac/ac converter. At the end of this mode, a half switching cycle is achieved.

The other six modes (**Modes 7–12**) corresponding to positive output current and output voltage and $V_{\rm sec} \leq 0$ can be explained following the explanations for Modes 1–6 and are illustrated in Fig. 4.

III. Results

The efficacy of the ZVS scheme is ascertained using open-loop-control experiments on the CHFL inverter topology (shown in Fig. 1). The results of the ZVS scheme are also compared with the conventional scheme for the ac/ac converter. The dc/ac converter operates at 20 kHz which transforms to a 40-kHz PWM frequency at the output of the secondary-side ac/ac converter due to frequency doubling. The rated power of the inverter is 1 kW while the input voltage is set at 36 V. For the dc/ac converter, OptiMOS power MOSFETs (IPP08CN10N G) from Infineon are used, which have with following key specifications: voltage and current ratings of 100 V and 95 A, respectively, gate charge of 100 nC, and ON-state resistance of 8.2 mΩ. For the ac/ac converter, Q-class HiPerFET power MOSFETs (IXFX21N100Q) from IXYS are used. The key specifications of this device are as follows: voltage and current ratings of 1000 V and 21 A, respectively; gate-to-source and gate-to-drain stored charges of 27 and 18 nC, respectively; and ON-state resistance of 0.5 Ω. A nanocrystalline core (STX 1060M1) is used for the center-tapped HF transformer with the number of primary and secondary turns being 12 and 104 (i.e., 2 × 52), respectively. The values of the output filter inductance (L_f) and capacitance (C_f) are set to be 2.4 mH and 0.5 μF, respectively.

Fig. 5 shows the comparison of the inverter efficiencies obtained using the ZVS and conventional schemes. The inverter efficiency using the ZVS scheme shows an improvement of over 2% at the rated power and over 3% at around 20% of the rated power. Fig. 6(a) and (b) shows the overlapping gate-to-source and drain-to-source voltages for the conventional and ZVS schemes, illustrating a softer discharge mechanism for the ZVS scheme. Fig. 7 shows the impact of the enhanced efficiency using the ZVS scheme on the output voltage of the inverter. The results of the open-loop inverter clearly show a higher output-voltage yield for the ZVS scheme as compared to that of the conventional scheme due to the enhanced efficiency obtained using the former. Finally, Fig. 8 compares the THD of the inverter output voltage using the ZVS and conventional schemes. The conventional scheme results in a small kink near the zero crossing. Hence, as the output power reduces and the switching effect becomes more dominant, the slight difference shows up as a small difference in the THD. However, at higher power, when the peak current is higher, the difference is negligible.

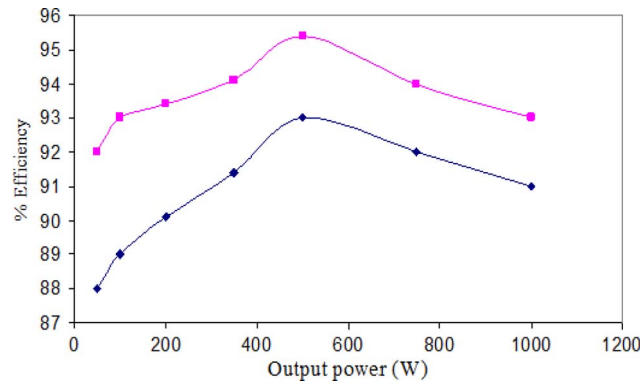

Fig. 5. Experimental comparison of the efficiencies of the (top trace) ZVS and (bottom trace) conventional schemes.

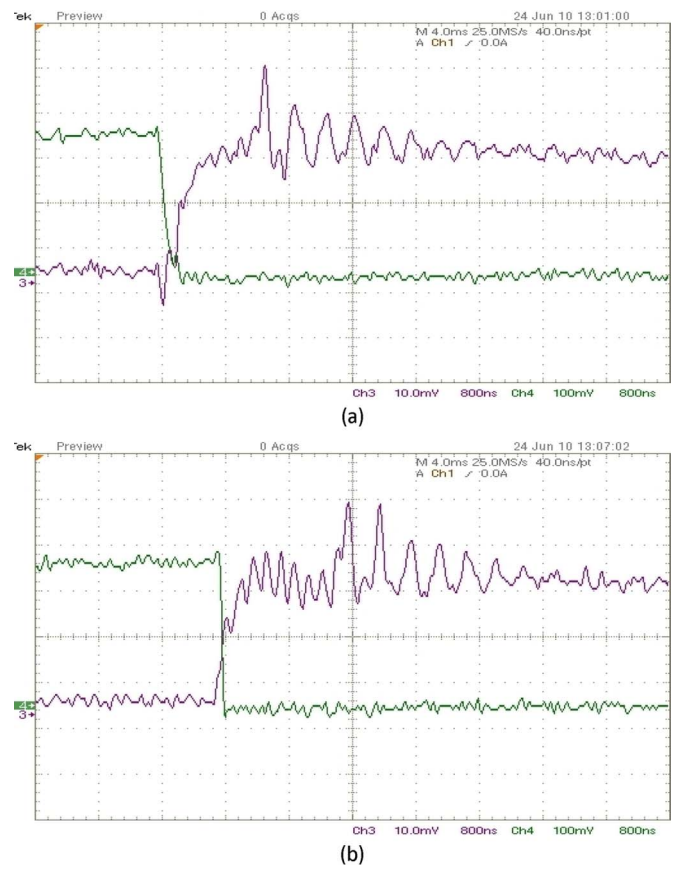

Fig. 6. MOSFET (falling trace) drain-to-source voltage and (rising trace) gate-to-source voltage for the ZVS and conventional schemes.

IV. Summary and Conclusion

A new ZVS scheme for the ac/ac converter of a CHFL inverter has been outlined in this letter. By mitigating the device

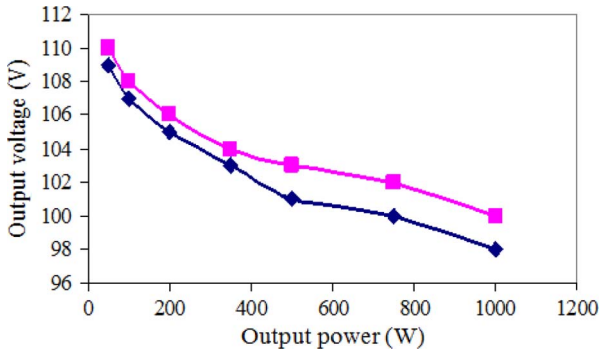

Fig. 7. Experimental output-voltage yield of the open-loop inverter with varying load demands for the (top trace) ZVS and (bottom trace) conventional schemes.

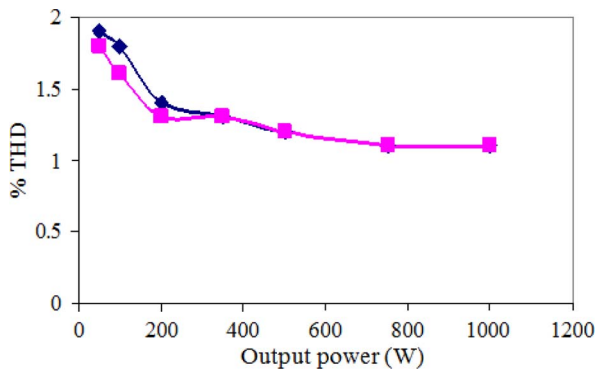

Fig. 8. Experimental THD of the inverter output voltage using the (bottom trace) ZVS and (top trace) conventional schemes.

switching loss, the ZVS scheme enables one to potentially choose power MOSFETs with lower ON-state resistance at the price of slightly higher output capacitance. Unlike the schemes outlined in [17]–[20], where a diode and an active device (e.g., MOSFET or IGBT) conduct during the transition and the ON-states, in the ZVS scheme, the diode only plays a small role during the transition. As such, the reverse recovery of the diode during the transition is reduced. These loss-mitigating mechanisms yield an improvement in the inverter (i.e., dc/ac converter followed by the ac/ac converter) efficiency of over 2% at the rated power and over 3% at around 20% of the rated power using the ZVS scheme. Aside from demonstrating the inverter efficiency using the ZVS scheme, we have also demonstrated the output-voltage yield and THD. They clearly show that a higher voltage and slightly better THD are yielded using the ZVS scheme due to higher efficiency and soft switching transition.

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