On Optimality of Adiabatic Switching in MOS Energy-Recovery Circuit

Baohua Wang and Pinaki Mazumder
Department of Electrical Engineering and Computer Science
The University of Michigan, Ann Arbor, MI 48109, USA
E-mail: {baohuaw, mazum}@eecs.umich.edu

ABSTRACT

The principle of adiabatic switching in conventional energy-recovery adiabatic circuit is generally explained in literature with the help of the rudimentary RC circuit driven by a constant current source. However, it is not strictly accurate to approximate MOS adiabatic circuit by such an elementary model since it fails to incorporate the nonlinearity of very deep sub-micron transistors. This paper employs the theory of variational calculus to extend the principle of optimality inherent in this RC model to general MOS adiabatic circuits. Our experimental results include energy dissipation comparison in various adiabatic schemes using optimal power clocking versus other waveforms.

Categories and Subject Descriptors: B.8.2 [Hardware]: Performance and reliability—Design Aids

General Terms: Design, Performance, Theory

Keywords: adiabatic circuit, power clocking, variational calculus

1. INTRODUCTION

Longer battery operating life is the cardinal goal in low-power VLSI design. However, conventional CMOS circuit styles are limited by constant power supply voltage that forces a significant portion of battery power being consumed as thermal energy in resistive circuit elements. In order to curtail this wasteful drainage of energy, innovative low-power energy-recovery adiabatic circuits were proposed in literature in order to replace the constant power supplies in traditional CMOS circuits by power clocks in the form of ramp or sinusoidal signals [3, 4]. The resulting adiabatic switching procedure achieves sub-$fCV_{DD}^2$ energy consumption due to aggressive reduction of resistive dissipation and also recycling of the stored energy in capacitive elements.

The principle of adiabatic circuit is usually illustrated by a RC circuit constructed by cascading a constant current source to represent the ramp power clock, a linear resistor $R_{eq}$ to model the resistive devices and the loading capacitor, $C_L$ [2]. The circuit energy consumption is given by

$$E = \xi^2 R_{eq} T, \quad \text{with} \quad I = C_L V_{DD}/T$$

(1)

where $T$ denotes the charging/discharging time, $V_{DD}$ is the voltage swing value, and $\xi$ is the shaping factor used to incorporate the other types of power clock waveform shapes than ramp waveform.

So far many adiabatic logic styles have been proposed, such as PAL, CAL, TSEL, SCAL, SCAL-D [8, 5, 6, 7]. Generally the operation of adiabatic logic gate is divided into two stages: one stage used for logic evaluation to produce the correct logic output value; the other stage used to reset the gate output logic value. Both the two stages utilize the principle of adiabatic switching implied in (1), i.e. the voltage drops through the resistive elements are made small to reduce their energy dissipation during charging/discharging loading capacitors. Fig. 1 shows two basic adiabatic logic gates, whose operating principles can be found from [1, 5]. Due to the nonlinearities exhibited by MOS transistors, the basic RC circuit used to illustrate the adiabatic switching principle shown by (1) is not akin to realistic MOS adiabatic circuit. In this work, we will discuss the impact of the nonlinear device properties on adiabatic circuit. Then we employ the theory of variational calculus to investigate the optimality of adiabatic switching, which answers how to achieve the best tradeoff between speed and energy dissipation in MOS adiabatic circuit.

The rest of the work is organized as follows. Section 2 shows the influences of devices characteristics on adiabatic circuit. Section 3 investigates the optimality of adiabatic switching using the theory of variational calculus. Section 4 presents the experimental results which include several adiabatic circuit applications using the optimal power clock versus other waveforms. Section 5 concludes this work.
Figure 2: The gate modelling.

2. GATE MODELLING

Before we discuss the adiabatic switching principle within the context of realistic MOS adiabatic circuit, in this section we introduce the gate and device modeling used in our analysis and show the impacts of devices properties on MOS adiabatic circuit.

To approximate the adiabatic logic gate, we use an abstract gate model shown in Fig. 2, where the power clock $V_{PC}$ drives the loading capacitor $C_L$ through a two-terminal block $G$. $G$ models the conducting transistor network in the modeled adiabatic logic gate. The power consumption of block $G$ is represented as $P_g(V_{PC}, V_{out})$, and the current for charging loading capacitor is denoted by $I_g(V_{PC}, V_{out})$. $V_{out}$ denotes the voltage level of the driven capacitor. For the consideration of generality, there is no KCL restriction applied to the gate model. Equation $P_g(\cdot) = (V_{PC} - V_{out})I_g(\cdot)$ does not always hold for the shown gate model.

2.1 The Influences of Device Properties

Since the adiabatic buffer shown in Fig. 1(a) is a typical representative of adiabatic circuit, we use it as an example to show the effects of device properties. Here we use the α-power law MOSFET model [9].

Without loss of generality, we consider the procedure of charging loading capacitor $C_L$ through the transmission gate (T-gate). In this procedure, the voltage drop through the drain and source of both PMOS and NMOS transistors can be considered as too small to saturate the transistors. Meanwhile the energy dissipation when the transistors in the linear conduction region will dominate the total energy consumption of the T-gate. Therefore it is reasonable that we analyze the energy dissipation of the T-gate by assuming transistors are in linear conduction region in this paper. In linear region, the equivalent conductances of PMOS and NMOS transistors using the α-power law model are given as

$$G_N = K_n(V_{DD} - V_{out} - V_{thn})^{\alpha_n/2}$$
$$G_P = K_p(V_{PC} - V_{thp})^{\alpha_p/2}$$

where $K_n$ and $K_p$ are the gains of the NMOS and PMOS transistors respectively. For the T-gate, we have $K_n = K_p = K$, $V_{thn} = V_{thp} = V_{th}$ and $\alpha_n = \alpha_p = \alpha$, assuming the T-gate is designed symmetrically.

When the velocity index $\alpha$ equals to 2, using the linearity of conduction, the lumped conductance of the T-gate defined by $G_T = G_N + G_P$ equals to $V_{dd} - 2V_{th} + (V_{PC} - V_{out})$. Using the first order approximation, we can say that $G_T$ has a constant value of $V_{dd} - 2V_{th}$. For the past MOS technology where the short-channel effects were not prominent, we can say this first order approximation was quite accurate at that time. Additionally the circuit speed was so low that the voltage drop of $V_{PC} - V_{out}$ through the T-gate can be neglected. This constant conductance approximation of T-gate was of central importance in [2], where discussions on optimizing adiabatic circuits were based on such an assumption. However this constant conductance approximation of T-gate is not very accurate now as device properties have changed.

Nowadays $\alpha$ is very close to 1 rather than 2, and also the adiabatic circuit speed is significantly improved due to the stronger drivability of transistors. These facts make it important to reconsider the applicability of the principle implied in (1) into adiabatic circuit design.

3. OPTIMAL ADIABATIC SWITCHING

In this section, we discuss the optimality of adiabatic switching for general MOS adiabatic circuit. We present a mathematical programming formulation for adiabatic switching based on the gate model shown in Fig. 2. The objective of the optimization problem is to determine what kind of power clock should be used in order to charge the loading capacitor from initial voltage $V_0$ to final voltage $V_T$ in the given time duration $T$, with the minimum energy dissipation by the gate. The mathematical formulation of the problem is given as:

Minimize $\int_0^T P_g(V_{PC}, V_{out})dt$  
\hspace{1cm} s.t. \hspace{0.5cm} V_{out}(0) = V_0, V_{out}(T) = V_T$

as well as satisfying the circuit equation given by

$C_L\frac{dV_{out}}{dt} = I_g(V_{PC}, V_{out})$.  

In this paper, $X$ or $\dot{X}$ is used to represent the derivative of variable $X$ with respect to time $t$.

Based on the theory in variational calculus[10], by introducing Lagrange multiplier $\lambda$, an equivalent program can be formulated as follows:

Minimize $\int_0^T Ldt$  
\hspace{1cm} s.t. \hspace{0.5cm} V_{out}(0) = V_0 \text{ and } V_{out}(T) = V_T$

where the Lagrangian, $L$, for the optimization problem is defined as

$L = P_g(V_{PC}, V_{out}) + \lambda \left( C_L V_{out} - I_g(V_{PC}, V_{out}) \right)$.  

The optimal conditions for the equivalent problem follow the theory in variational calculus, i.e. the variables in the lagrangian of the variational calculus problem like (5) should satisfy the Euler-Lagrange equation:

$$\frac{\partial L(X, \dot{X})}{\partial X} - \frac{d}{dt} \left[ \frac{\partial L(X, \dot{X})}{\partial \dot{X}} \right] = 0$$

where $X$ is any unknown variable in $L$.

3.1 The Optimal Conditions

By applying the Euler-Lagrange equation (7) to variable $V_{PC}$ for $L$ defined by (6), part of the optimal conditions for (5) can be given as

$$C_L\dot{\lambda} = \frac{\partial P_g}{\partial V_{PC}} - \lambda \frac{\partial I_g}{\partial V_{out}} - \frac{\partial P_g}{\partial V_{out}} - \lambda \frac{\partial I_g}{\partial V_{PC}} = 0$$

\hspace{1cm} (8)

\hspace{1cm} (9)
For variable \( \lambda \), by applying (7), we exactly obtain the circuit equation given by (4).

Using (9) and applying chain rule that

\[
\dot{\lambda} = \frac{\partial \lambda}{\partial V_{PC}} \dot{V}_{PC} + \frac{\partial \lambda}{\partial V_{out}} \dot{V}_{out}
\]

to (8), we have

\[
\frac{\partial \lambda}{\partial V_{PC}} (C_L \dot{V}_{PC}) + \frac{\partial \lambda}{\partial V_{out}} (C_L \dot{V}_{out}) = \frac{\partial P_g}{\partial V_{out}} - \frac{\partial P_g}{\partial V_{PC}} \cdot \left( \frac{\partial \lambda}{\partial V_{out}} \right) / \left( \frac{\partial \lambda}{\partial V_{PC}} \right)
\]

(10)

Using circuit equation (4), dividing the left hand side (LHS) of (10) by \( C_L \dot{V}_{out} \) and dividing the right hand side (RHS) of (10) by \( I_g(t) \), and applying chain rule that

\[
\frac{dV_{PC}}{dt} = \left( \frac{dV_{pc}}{dt} \right) / \left( \frac{dV_{out}}{dt} \right) = V_{PC} \frac{dV_{PC}}{V_{out}}
\]

we can obtain the following differential equation with respect to \( V_{PC} \) and \( V_{out} \) as

\[
\frac{dV_{PC}}{dV_{out}} = \left( \frac{1}{I_g} \cdot \frac{\partial P_g}{\partial V_{out}} - \frac{\partial \lambda}{\partial V_{PC}} \right) / \left( \frac{\partial \lambda}{\partial V_{PC}} \right) = \frac{1}{I_g} \cdot \frac{\partial P_g}{\partial V_{out}} - \frac{\partial \lambda}{\partial V_{PC}}
\]

(11)

3.2 The Optimality of Adiabatic Switching

Since \( \lambda \) depends only on \( V_{PC} \) and \( V_{out} \) as seen from (9), by defining the RHS of (11) as a function given by \( A(V_{out}, V_{PC}) \), we have the following theorem:

**Theorem 1.** In the process of switching \( V_{out} \), the optimal adiabatic switching is governed by

\[
\frac{dV_{PC}}{dV_{out}} = A(V_{out}, V_{PC}^{opt})
\]

(12)

where \( V_{PC}^{opt} \) denotes the optimal power clock, and \( A(\cdot) \) is completely determined by the device properties.

According to Theorem 1, we can note that although in the optimal adiabatic switching procedure, the output voltage \( V_{out} \) and the power clock \( V_{PC} \) are transient signals, i.e. functions of time \( t \), time does not play a role in the relation between \( V_{PC} \) and \( V_{out} \). In other words, the optimal power clock voltage \( V_{PC}^{opt} \) at time instant \( t \) can be determined if the output voltage value \( V_{out} \) is known at that time, no matter what \( t \) is, i.e.

\[
V_{PC}^{opt}(t=t_0) = V_{PC}^{opt}(V_{out}(t_0)), \quad \text{for any } t_0
\]

(13)

However in order to determine \( V_{PC}^{opt}(V_{out}) \) for \( V_0 < V_{out} \leq V_T \) from (12), one initial voltage value for \( V_{PC}^{opt} \) is required, in other words we need know the value of \( V_{PC}^{opt} \) at \( V_{out} = V_0 \). Thus we can represent the optimal power clock with such a function as

\[
V_{PC}^{opt}(V_{out}) = F(V_{out}, V_{PC}^{opt}(V_0)),
\]

(14)

where the initial voltage \( V_{PC}^{opt}(V_0) \) is determined by time duration \( T \), loading capacitance \( C_L \) and device properties.

Applying Theorem 1 to the basic RC adiabatic circuit used by (1), we can draw the following conclusion:

**Conclusion 1.** From Theorem 1, for basic RC adiabatic circuit, (1) shows the minimum amount of energy consumption and the constant current source gives the best power clock source.

The optimality of the principle implied by (1) is evident according to Theorem 1.

3.3 Solving the Optimal Conditions

To obtain the optimal power clock waveform for problem (3), we first characterize \( A(V_{out}, V_{PC}^{opt}) \), which depends only on device properties. According to Theorem 1, using any initial guess of \( V_{PC}^{opt}(V_0) \), we can get an optimal power clock curve \( V_{PC}^{opt}(V_{out}) \) by solving (12). Applying such an optimal power clock waveform to the circuit equation (4), we can obtain \( V_{out}(T) \), the output voltage at time \( T \). If \( V_{out}(T) \) equals to \( V_T \), then we have obtained the optimal power clock. Otherwise the initial value, \( V_{PC}^{opt}(V_0) \) need be revised, (12) need be solved again and the obtained new optimal power clock curve need be applied to circuit equation (4) again. The procedure is repeated until an appropriate optimal power clock curve is found such that the capacitor is charged to \( V_T \) at time \( T \).

\( F(x) \) in (14) can be calculated by solving (12) with any given value of \( V_{PC}^{opt}(V_0) \). Therefore the iterative procedure can be speeded up by using methods like lookup tables to pre-characterize \( F(V_{out}, V_{PC}^{opt}(V_0)) \) only once with respect to different values of \( V_{PC}^{opt}(V_0) \) and \( V_{out} \). Based on such types of pre-characterization, the iterative procedure for deriving the optimal power clock is given as follows:

**Algorithm Opt_PC**

Begin

a. Set the initial guess of \( V_{PC}^{opt}(V_0) \)

\[
V_{PC}^{opt}(V_0) = \frac{R_{eq}C_LV_T}{T},
\]

where \( R_{eq} \) is an estimation of the driving resistance for the given adiabatic circuit.

b. Use \( V_{PC}^{opt}(V_{out}) \) as the power clock source to simulate the adiabatic circuit. \( V_{PC}^{opt}(V_{out}) \) is modeled as a voltage controlled voltage source, whose property is determined by the constructed lookup table for \( F(V_{out}, V_{PC}^{opt}(V_0)) \)

c. With the applied power clock waveform, if the simulated output voltage of the loading capacitance at time \( T \) is close to \( V_T \) within acceptable error tolerance, the transient profile of \( V_{PC} \) during this simulation is the optimal transient power clock waveform.

d. Otherwise update \( V_{PC}^{opt}(V_0) \) using recurrence formulas as in Newton-Raphson method and go to Step b.

End

4. EXPERIMENTAL RESULTS

4.1 NMOS TSEL Inverter Example

We use the gate reseting stage for the NMOS TSEL inverter shown in Fig. 1 as an example. When \( V_{PC} > V_{th} + V_A \), supposing \( V_{in} = V_D^{opt} \) and \( V_{out} = 0 \) at that time, power clock \( V_{PC} \) tries to pull up the voltage at node \( out \). On the other
hand the reference voltage \( V_R \) tries to pull down the voltage at node \( \text{out} \). In the duration before \( N_1 \) goes into linear region, \( N_1 \) and \( N_3 \) will undergo several regions. In this duration, the abstract gate model shown in Fig. 2 is suitable despite that traditional 2-terminal devices can not describe the relation between the inverter's total power consumption and its output current for driving the load capacitors. Hspice simulation is used to characterize the gate directly and find out the optimal power clock waveform using algorithm \( \text{Opt}_{PC} \).

Fig. 3 shows the simulation results using different waveforms. Case "Sin" shows the conventional sinusoidal power clock situation, where \( N_3 \) begins going into linear region at time instant 1.66ns. In both cases of "Opt1" and "Opt2", the optimal waveform is applied in the duration before this time instant. For case \( \text{Opt1} \), we use a ramp input from 1.48V to 2.7V after 1.66ns. In case \( \text{Opt2} \), we use two ramps after 1.66ns. The energy dissipation in the duration when the optimal waveform is used, i.e. before time instant 1.66ns, is 2.79fJ(65.8%), in contrast to that of 8.17fJ(0%) for case \( \text{Sin} \). The percentages show the improvement on energy dissipation compared to the case where zero percentage is indicated. The total energy dissipation from 0 to 2.5ns is as follows: 107.9fJ(0%) for case \( \text{Sin} \), 60.6fJ(43.8%) for case \( \text{Opt1} \) and 43.6fJ(39.5%) for case \( \text{Opt2} \). The overall waveform in case \( \text{Opt2} \) which leads to the lowest energy dissipation in this example is more like a mirrored version to the sinusoidal power clock with respect to its diagonal.

### 4.2 Comparison to Stepwise Charging

Fig. 4 shows the Hspice simulation results for driving a 5pF capacitor in a time duration of 5ns using a \((35 \times 1)\)-NMOS transistor in 0.18\(\mu\)m technology under different power supply conditions. In the figure, "Optimal" indicates the case of using the optimal power clock, which is obtained from algorithm \( \text{Opt}_{PC} \), and the used \( A(\cdot) \) for solving (12) is obtained directly from Hspice simulation; "Step" denotes the case of stepwise charging [11]; "Ramp" means the case of using ramp power clock where the ramp starting point is chosen such that at 5ns, the output voltage is very close to the output produced by using constant power supply; "Constant" denotes the constant power supply situation where \( V_{DD} = 3.3V \).

Because the effect of stepwise charging is not prominent in the final step, we only compare the energy dissipation in the
duration of the first two steps, which is 3.2ns. The energy dissipation in case \( \text{Step} \) is 5.96pJ(77.9%), that in case \( \text{Optimal} \) is 4.97pJ(81.6%), that in case \( \text{Ramp} \) is 6.37pJ(76.4%), and that in case \( \text{Const} \) is computed analytically as 27pJ(0%). It is obvious that the optimal power clock naturally leads to the minimum energy dissipation.

### 5. CONCLUSIONS

By employing variational calculus, this paper extends the optimality of adiabatic switching for basic \( RC \) adiabatic circuit to general energy-recovery MOS circuits. It also demonstrates the effects of the optimal power clock waveforms on several adiabatic circuit applications. The mathematical model discussed in this paper provides certain insights into the relation between the energy dissipation and the circuit speed for general adiabatic circuit.

### 6. REFERENCES


---

**Figure 3: NMOS TSEL inverter under various power clock waveforms.**

**Figure 4: Comparisons of using various types of waveforms to drive a large capacitive load.**